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<u>REMARKS</u>

<u>Rejection of Claims 1-3, 5, and 14 Under 35 U.S.C. §102(e) based on *Borland* (U.S. Patent No. 6,219,824).</u>

5   The invention of amended claim 1 is directed to an integrated circuit device that includes a programmable portion with a plurality of circuits that may be configured by a user of the integrated circuit device. The integrated circuit device also includes at least one communication portion. The communication portion includes at least one circuit block manufactured to perform a predetermined data communication function including converting received first data values into
10   second data values.

          As is well known, a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single reference.

          The cited reference *Borland* does not teach at least one communication portion with a circuit block that converts received first data values into second data values. *Borland* teaches an
15   integrated circuit with input/output (I/O) programmable logic. Such an integrated circuit also has other portions, including a main functional unit, a memory, and a direct memory access (DMA) controller.[1] However, these other portions are never described as including, expressly or inherently, a circuit block as recited in claim 1.

          A main functional unit of *Borland* is described as ranging from a processor to an
20   interconnected system of processing modules.[2] While various functions for the main functional unit are mentioned, conversion of data values is not described or suggested.[3] Thus, the main functional unit of *Borland* does not show or suggested a circuit block as set forth in claim 1.

          The remaining sections of the integrated circuit of *Borland* do not show or suggest all limitations of claim 1, either. The DMA controller of *Borland* is described only as fulfilling I/O
25   requests.[4] Similarly, the I/O programmable logic of *Borland* is described only as controlling

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[1] See *Borland*, FIG. 2, which shows main functional unit 200, memory 210, DMA controller 220 and I/O programmable logic unit 230.
[2] See *Borland*, Col. 3, Lines 60-63.
[3] See *Borland*, Col. 3, which describes the function of: computing functions for fulfilling an I/O request, reading and storing configurations programmable I/O logic, programming the programmable logic, and program and operate a DMA controller from a memory. No mention of made of converting data values.
[4] See *Borland*, Col. 4, Lines 24-26.

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transmission of data to and from I/O pads, and thus does not show or suggest data conversion.[5] Finally, the memory of *Borland* is described as storing a number of configurations for I/O programmable logic, without mention of any data conversion.[6]

     Accordingly, because, none of the integrated circuit elements of *Borland* shows all the

5   limitations of amended claim 1, this ground of rejection is traversed.

     Claim 2, which depends from claim 1, includes additional limitations not shown in the cited reference. Claim 2 adds that a programmable portion comprises a programmable interconnect portion and a logic gate portion. *Borland* describes an integrated circuit that may include conductive lines and transistors.[7] However, such teachings are evidence of some sort of

10   interconnect, but do not show a <u>programmable</u> interconnect portion, as clearly recited in claim 2. Clarification of where such a limitation is shown in the references is respectfully requested.

     For all of these reasons, the rejection of claims 1-3, 5, and 14 is traversed.

<u>Rejection of Claim 4 Under 35 U.S.C. §103(a) based on *Borland* in view of *Jefferson* (U.S.</u>

15   <u>Patent No. 6,127,865).</u>

     Claim 4, which depends from claim 1, adds a timing circuit that receives a clock signal and generates an internal clock signal. The internal clock signal is phase shifted with respect to the clock signal.

     As is well understood, to establish a prima facie case of obviousness, a rejection must

20   meet three basic criteria. First, there must be some suggestion or motivation to modify a reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference(s) must teach or suggest all claim limitations.

     To the extent that this rejection relies on *Borland*, the comments set forth above for claim 1 are incorporated by reference herein. Namely, that *Borland* does not show at least one circuit

25   block manufactured to perform a predetermined data communication function including converting received first data values into second data values.

     Such a limitation is also lacking from the remaining cited reference *Jefferson*. *Jefferson* is directed to a delay compensated clock signal for a programmable logic device. The reference does not show or suggest a communication portion with a circuit block as recited in claim 1. In

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[5] See *Borland*, Col. 4, Lines 19-21.
[6] See *Borland*, Col.

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fact, *Jefferson* is believed to teach away from the invention, as it represents a conventional case in which a PLD includes programmable logic circuits, and does not dedicate particular circuit blocks to predetermined functions,[8] like the data communication functions as recited in claim 1.

Accordingly, because the combination of *Borland* in view of *Jefferson* does not show all the limitations of claim 4, this ground for rejection traversed.

Rejection of Claim 12 Under 35 U.S.C. §103(a) based on *Borland* in view of *Jefferson* and further in view of *Reddy et al.* (U.S. Patent No. 5,942,914).

Claim 12, which depends from claim 6, adds the limitation that each communication portion includes a data multiplexer (MUX) that enables a data path between one of a plurality of inputs and a data MUX output, each data operation circuit being coupled to an <u>input</u> of the data MUX.

It is admitted that the references *Borland* and *Jefferson* do not show or suggest a data MUX.[9] However, such a limitation is not shown in last reference *Reddy et al.*, either.

According to claim 12, each data operation circuit is coupled to an <u>input</u> of a data MUX. Thus, the invention of claim 12 recites an arrangement in which two data operation circuits can provide input values to a data MUX. This is in sharp contrast to *Reddy et al.*, which shows multiplexers having inputs connected to global conductor lines and outputs connected to logic array blocks (LABs).[10] In short, *Reddy et al.* teaches multiplexers that <u>provide data to</u> circuit portions (e.g., LABs), while Applicants' claim 12 recites an arrangement in which a data MUX can <u>receive data from</u> data operation circuits.

Accordingly, because the cited reference does not show or suggest all limitations of claim 12, this ground for rejection is traversed.

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[7] See *Borland*, Col. 3, Lines 21-34.
[8] See *Jefferson*, FIG. 2, which shows a PLD having numerous programmable portions, but no portions dedicated to providing any particular function, let alone a data communication function.
[9] See the Office Action, dated 7/3/02, Page 4, Lines 9-12.
[10] See *Reddy et al.*, FIG. 5, which shows global conductor lines 302 connected to inputs of multiplexers 306. Outputs of multiplexers 306 are connected to LABs.

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Claim 1 has been amended. The present claims 1-23 are believed to be in allowable form. It is respectfully requested that the application be forwarded for allowance and issue.

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Respectfully Submitted,

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Version With Markings to Show Changes Made

In the Claims.

5   1. (Amended) An integrated circuit device, comprising:

a programmable portion comprising a plurality of circuits that may be configured by a user of the integrated circuit device; and

at least one communication portion comprising at least one circuit block manufactured to perform a predetermined data communication

10   function **including converting received first data values into second data values**.

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